BARROT

BR8654A02

Datasheet

October 9, 2023

Version 1.1

VERSION HISTORY

Revision	Amendment	Date	Author
1.0	Initial Version	2023-06-12	Daniel
1.1	Update The Features page	2023-10-09	Asher

Contents

General Description

BR8654A02 is Bluetooth 5.4 SOC. A highly integrated SOC for Bluetooth data stream process, BR8654A02 integrates a low power MCU, RF transceiver, Baseband, Modem, USB Device, SARADC and up to 16 GPIOs in a single chip. BR8654A02 offers low cost, low power consumption, flexible and more powerful Bluetooth application.

BR8654A02 operates with a widely IO power supply range from 1.8V to 3.3V and has very low power consumption in both TX and RX modes, enabling long lifetimes in battery-powered systems while maintaining excellent RF performance. The device can enter an ultra-low power sleep mode in BT sniff mode and BLE connection interval.

Features

- Support Bluetooth v5.4 specification compliant
- 32-bit RISC processor up to 96MHz with on-chip ROM(384Kbytes) and RAM(96Kbytes)
- Operating temperature：-40°C to +125°C
- 1.8V to 3.3V IO power supply
- Integrated 5V LDO
- Various internal memory resources (512Kbytes flash) support custom own software code development
- Power modes included shutdown/deep sleep/light sleep/active
- Wake up by UART/GPIO(sleep), and RTC(deep sleep)
- Package: QFN32 5*5
- Low level Bluetooth protocols embedded (LL/LMP, L2CAP, RFCOMM, SDP, etc.)
- Support the Bluetooth smart firmware includes Security Manager(SM), Attribute Protocol(ATT), the Generic Attribute Profile(GATT) and Generic Access Profile(GAP)
- High speed UART or USB port for BT HCI and AT commands
- High speed UART port for BT HCI and Data interface, up to 4Mbps
- Support secure connection with AES-128
- Support up to 7 ACLs and 2 SCO/eSCO link for BR/EDR.
- Support up to 4 BLE links (Up to 3 links in slave mode).
- Single pin RF connection (50 ohm impedance in TX and Rx mode)
- High performance on-chip RF transceiver with integrated balun
- Integrated Power amplifier with maximum +6dbm transmit power output, support Bluetooth class 1.5 application without external PA
- Integrated external PA controller
- Support LE 1M/2M/Coded PHY and BR/EDR
- Up to +6dBm RF transmit power
- GFSK/π/4-DQPSK/8DPSK modulator
- GFSK/π/4-DQPSK/8DPSK demodulator
- RF/Analog Control (AGC, PA, Ramp up/down timer, Low power)
- Embedded high speed and low power CPU with on-chip ROM(384Kbytes) and RAM(96Kbytes)
- Embedded 8 channel 12bit 375kHz sps SARADC for

peripheral controls
- Embedded PGA for SARADC
- Built-in PLL, support system run up to 96MHz, and built-in crystal oscillator 24MHz
- Embedded PMU for efficient power management
- I2C master/slave, support standard and fast mode
- 4 sets PWM interface
- 4-wire SPI(master and slave) interface, up to 12MHz
- Audio interface: I2S up to 12MHz
- 8x channels DMA for peripheral interface (UART,USB,I2C,SPI)
- WDT/RTC/8x Timers
- 2x UARTs (uart0 has CTS/RTS)
- Various (total 16) GPIOs for various purposes
- Embedded SPI flash support XIP mode, Facilitate customer application development
- Support firmware upgrade over SWD/UART/USB or Air(OTA)

Applications

- Standard HCI defined by SIG
- Printer
- Bluetooth HID
- Smart home
- TV remote controller
- Toys
- Mesh network
- Data communication application

1. Chip Block Diagram

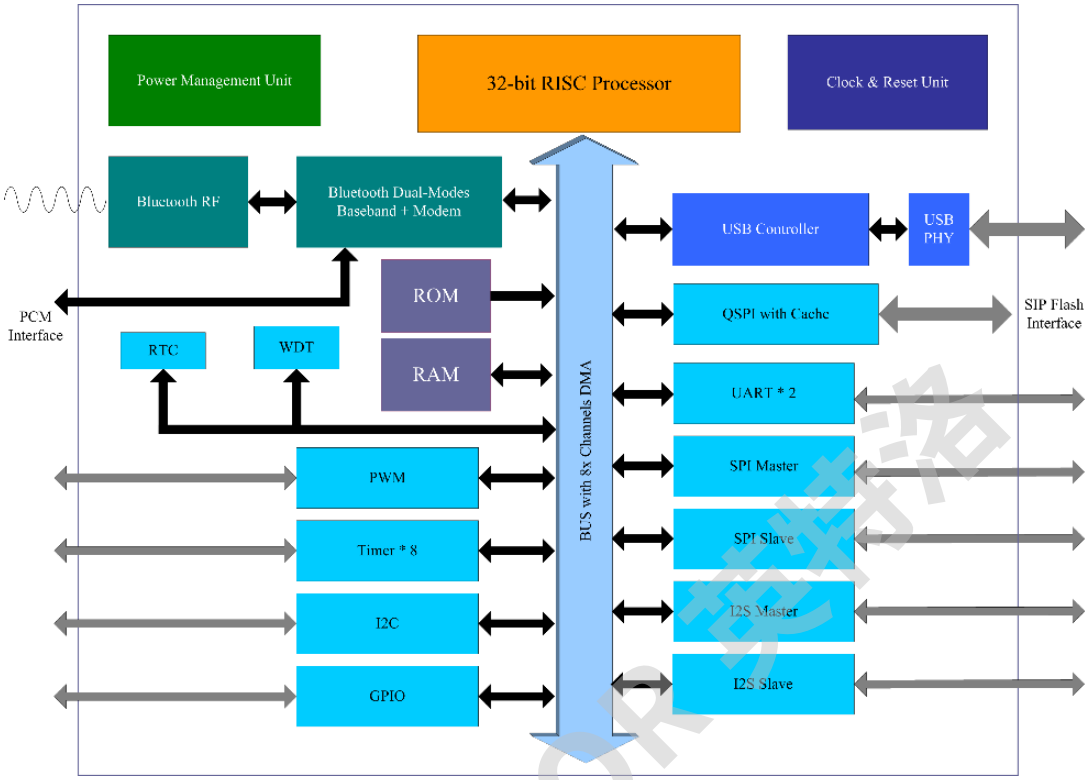

Figure 1: BR8654A02 Functional Block Diagram

2. PIN Diagram

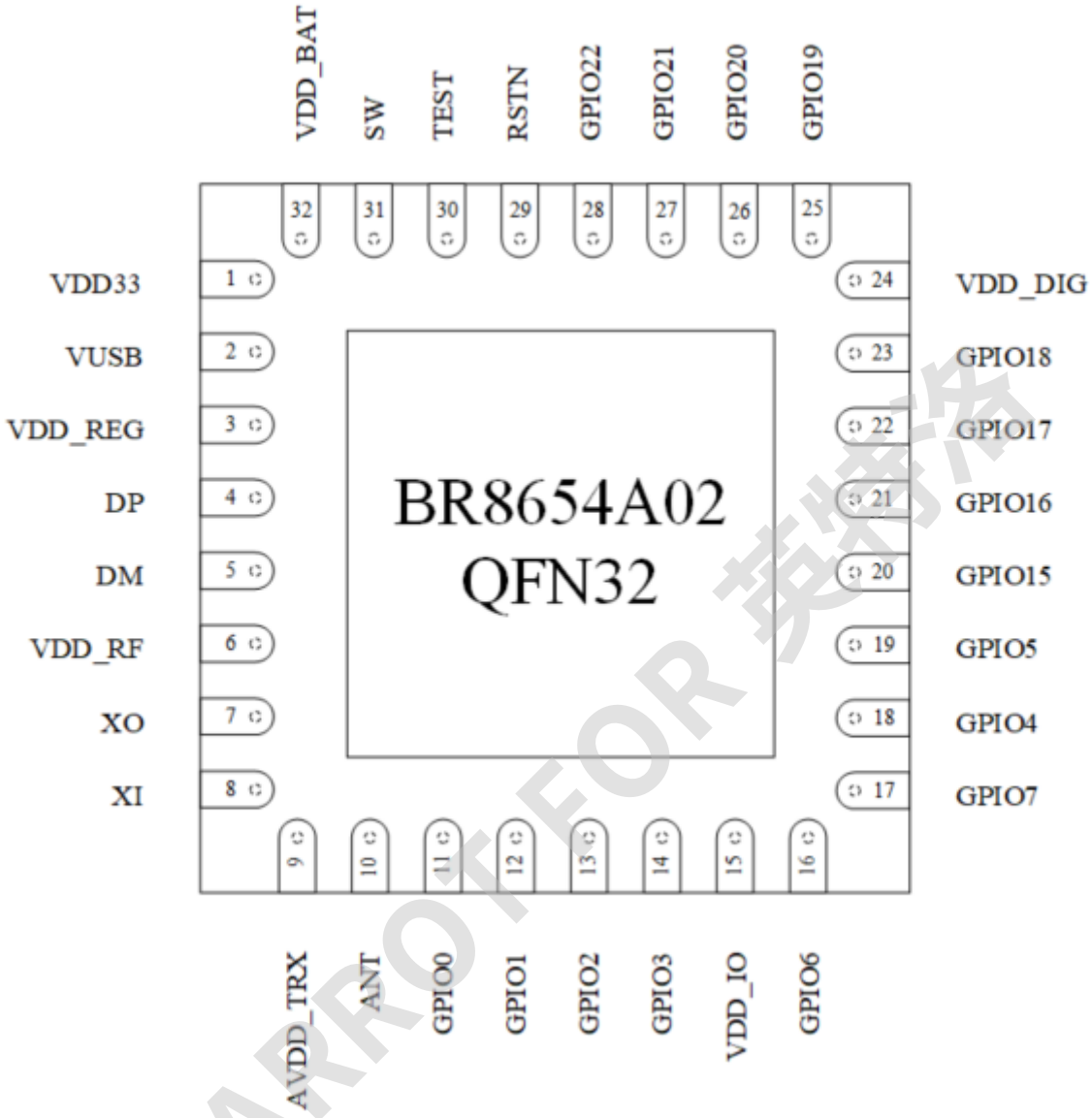

Figure 2: QFN32 Package PIN Diagram

3. PIN Assignment

3.1. Pin Description

BR8654A02 is a CMOS device. Floating level on input signals will cause unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Table 1 BR8654A02 PIN Notation Description

Notation	Description
I	Input
O	Output
IO	Bidirectional
OD	Open Drain
P	Power
G	Ground

Table 2 BR8654A02 Pin Description

Pin Name	No.	IO Type	Description
VDD33	1	P	USB LDO output pin, The output voltage is 3.3V
VUSB	2	P	USB LDO input pin, The input voltage is 5V
VDD_REG	3	P	1.6V RF LDO and 1.2V Core LDO input pin
DP	4	IO	USB DP data
DM	5	IO	USB DM data
VDD_RF	6	P	1.6V RF LDO output pin
XO	7	O	24M crystal output pin
XI	8	I	24M crystal input pin
VDD_TRX	9	P	1.6V RF system voltage input pin
ANT	10	IO	2.4GHz RF input output pin
GPIO0	11	IO	General purpose input/output, default is UART0_TX

GPIO1	12	IO	General purpose input/output, default is UART0_RX
GPIO2	13	IO	General purpose input/output, default is UART0_RTS
GPIO3	14	IO	General purpose input/output, default is UART0_CTS
VDD_IO	15	P	3.3V IO voltage input pin
GPIO6	16	IO	BOOT Mode
GPIO7	17	IO	General purpose input/output, default is GPIO
GPIO4	18	IO	General purpose input/output, default is SWCLK
GPIO5	19	IO	General purpose input/output, default is SWDIO
GPIO15	20	IO	General purpose input/output, default is GPIO
GPIO16	21	IO	General purpose input/output, default is GPIO
GPIO17	22	IO	General purpose input/output, default is GPIO
GPIO18	23	IO	General purpose input/output, default is GPIO
VDD_DIG	24	P	Digital CORE LDO 1.2V output pin
GPIO19	25	IO	General purpose input/output, default is GPIO
GPIO20	26	IO	General purpose input/output, default is GPIO
GPIO21	27	IO	General purpose input/output, default is GPIO
GPIO22	28	IO	General purpose input/output, default is GPIO
RSTN	29	I	SOC RESET PIN
TEST	30	I	Test mode enable pin
SW	31	IO	DCDC switch pin

VDD_BAT	32	P	Battery voltage 3.3V input pin

3.2. Package Pin Assignment

Table 3 BR8654A02 PIN Assignment

PIN name	Function0 mode	Function1 mode	Function2 mode	Function3 mode
GPIO0	UART0_TX	GPIO	TX_EN	UART0_TX(output)
GPIO1	UART0_RX	GPIO	RX_EN	UART0_RX (input)
GPIO2	UART0_RTX	GPIO	PWM1	N/A
GPIO3	UART0_CTX	GPIO	PWM2	N/A
GPIO6	BOOT Mode	N/A	N/A	N/A
GPIO7	GPIO7	CLK_EXT_32K_IN(ext clock source)	PWM1	N/A
GPIO4	SWD_CLK	GPIO	PWM3	I2C_SCLK
GPIO5	SWD_DIO	GPIO	PWM4	I2C_SDA
GPIO15	GPIO	UART1_TX	SPIM_CLK	SPIS_CLK
GPIO16	GPIO	UART1_RX	SPIM_CSN	SPIS_CSN
GPIO17	GPIO	I2C_SCLK	SPIM_MISO	SPIS_MISO
GPIO18	GPIO	I2C_SDA	SPIM_MOSI	SPIS_MOSI
GPIO19	GPIO	(BB)PCM_CLK	I2S_CLK	UART1_TX
GPIO20	GPIO	(BB)PCM_SYNC	I2S_FS	UART1_RX

GPIO21	GPIO	(BB)PCM_IN	I2S_IN	TX_EN
GPIO22	GPIO	(BB)PCM_OUT	I2S_OUT	RX_EN

4. Functional overview

4.1. UART Interface

It supports both HCI and Data mode on BR8654A02 and the features as below:

- Support hardware flow control.
- Support fractional baud rate.
- Support speed of up to 4Mbit/s.
- UART0 can be served by the DMA controller.

4.1.1. Port description

Table 4 Four-wire serial bus interface

UART_TX	serial data out
UART_RX	serial data in
UART_RTS	request to send
UART_CTS	clear to send

4.2. USB Interface

Support USB 2.0 full speed mode.

4.3. SPI Interface

There are 2 SPIs that one is in master mode and the other is in slave mode, with speed up to 12MHz. Both can be served by the DMA controller.

4.4. QSPI Interface

The Quad SPI can support 1/2/4-lines flash memory, with speed up to 24MHz. It can be served by the DMA controller.

4.5. I2C Interface

The I2C bus interface can operate in master or slave mode. They both can support standard and fast mode, and can be served by the DMA controller.

4.6. I2S Interface

The I2S bus interface can operate in master or slave mode. It can only handle audio data transmission, with a speed up to 12MHz.

4.7. DMA

The DMA is supported for 8-channels, 16 requests. It can manage memory-peripheral, peripheral-memory and memory-memory transfers. It can be used with peripherals: UART0, SPI, QSPI, I2C, USB.

4.8. Timers

Timers x8 with 32-bits width

4.9. RTC

N/A

4.10. WDT

32-bits counter width

4.11. ADC Characteristics

Tc = 27℃, VDD = 1.2V.

Table 5 ADC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT

Input voltage range	-	0	-	3.3	V
Resolution	-	-	12	-	Bits
Sample rate	-	93.75	375	750	ksps
ENOB	375ksps, 17kHz 1.1V Vpp input tone	-	11.57	-	Bits
THD		-	-70	-	dB
SINAD		-	65	-	dB
SFDR		-	70	-	dB
Conversion time	Time-to-output, 24MHz clock	-	64	-	Clock-cycles
Current consumption	Continue-sample mode	-	0.24	-	mA
Reference voltage	-	-	1.2	-	V

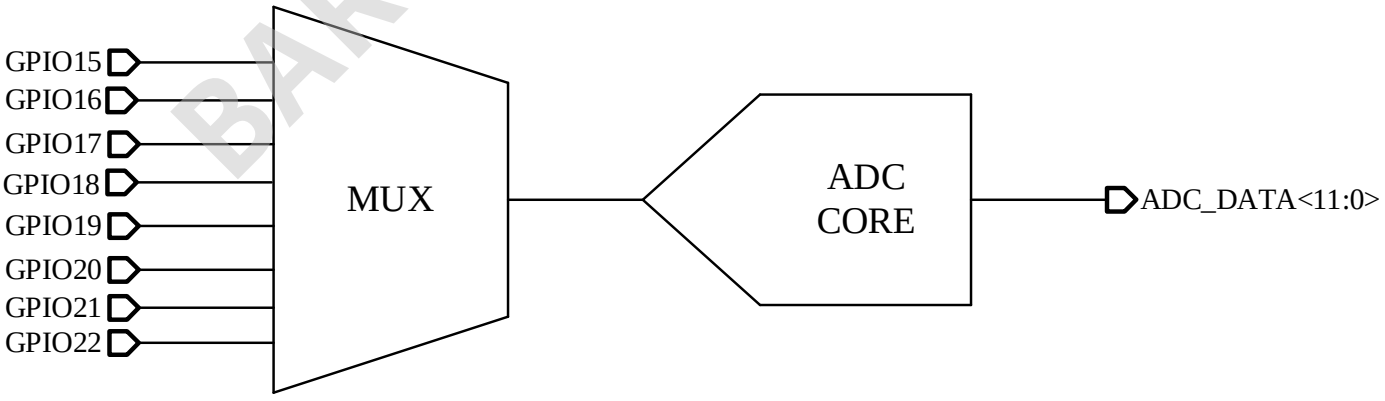

Figure 3 ADC signal path

5. Audio Interfaces

BR8654A02 has a digital audio interface that is a PCM interface.

5.1. PCM Interface

The audio PCM interface on the BR8654A02 chip features:

Operating at variable frequency (i.e. PCM master clock)

Table 6 PCM interface

Bus master or Bus Slave operation	-
8kHz PCM frame rate	-
Supports physical PCM format (single-clocking) at the following bit rates:	-
128kbps	16 bits/frame
256kbps	32 bits/frame
512kbps	64 bits/frame
1.024Mbps	128 bits/frame
2.048Mbps	256 bits/frame
4.096Mbps	512 bits/frame

Several PCM data output driver options:

- push-pull, always driven
- push-pull, hi-Z outside active slots
- open-drain
- Five different frame sync pulse shapes:
  - encloses last falling PCMCLK edge (Mono Codec)
  - encloses first rising PCMCLK edge (Mono Codec)
  - encloses first falling PCMCLK edge (Mono Codec)
  - encloses first eight bits in the frame (Mono Codec)
  - encloses first sixteen bits in the frame (Mono Codec)
- Transparent access to any contiguous byte-aligned 32bits in the frame (configurable first active slot)

- Audio level setting for Motorola audio codecs supported
- Support for one 13, 14, 16bit linear audio codecs or two 8bit A/μ-law PCM codec

Generic hardware data (DPV, direct PCM voice) interface for other data handling modules:

- Bluetooth CVSD transcoder
- Hardware A/μ-law transcoder if required
- FIFOs, if extensive software algorithms have to be applied to the exchanged data samples
- Hardware protocol handler (e.g. for IOM2 monitor channel)
- Up to two slots (i.e. 2*8 bit) directly connected to hardware data interface (CVSD transcoder), two other slots

connected to simple register

- 8kHz clock interface to synchronize timing in PCM master mode / output received timing in slave mode
- DPLL guarantees smooth timing correction (154ppm/166ppm, depending on pcm_gclkclock frequency)

5.1.1. Port description

Table 7 Four-wire serial bus interface

PCM_CLK	clock
PCM_SYNC	frame sync (mono)
PCM_IN	serial data in
PCM_OUT	serial data out

5.1.2. Timing

A typical example for the PCM port configuration is given in the timing diagrams below:
Settings for PCM mode sample timing diagram

- Frame sync: last falling edge
- Sample data size: 13bit
- Enabled slots: 0 and 1

- First active slot configured is 0
- PCMDOUT: tri-state outside transmission

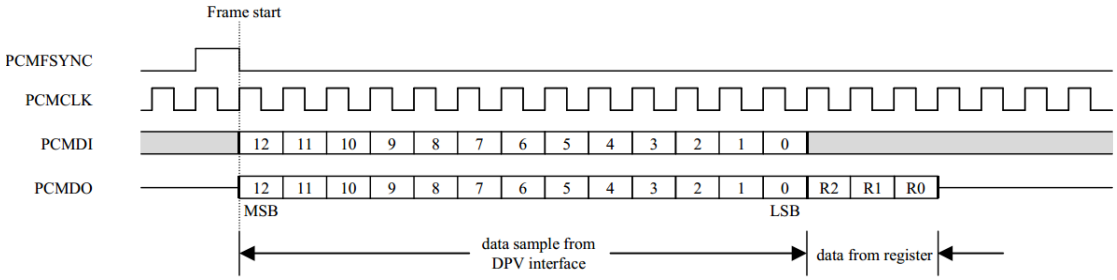

Figure 4: Basic Port Timing Diagram Example (PCM Mode)

6. Electrical Characteristics

6.1. Power Supply DC Characteristics

Table 8 BR8654A02 Power DC Characteristics

Symbol	Parameter	Units	Min	Typical	Max
VUSB	USB supply voltage	V	4.5	5	5.5
VBAT	Battery supply voltage	V	1.9	3.3	3.63
VDD_DIG	1.2V Digital CORE LDO output voltage	V	0.9	1.2	1.32
VDD_TRX	RF power supply voltage	V	1.5	1.6	1.8
VDD_IO	IO power supply	V	1.8	3.3	3.63

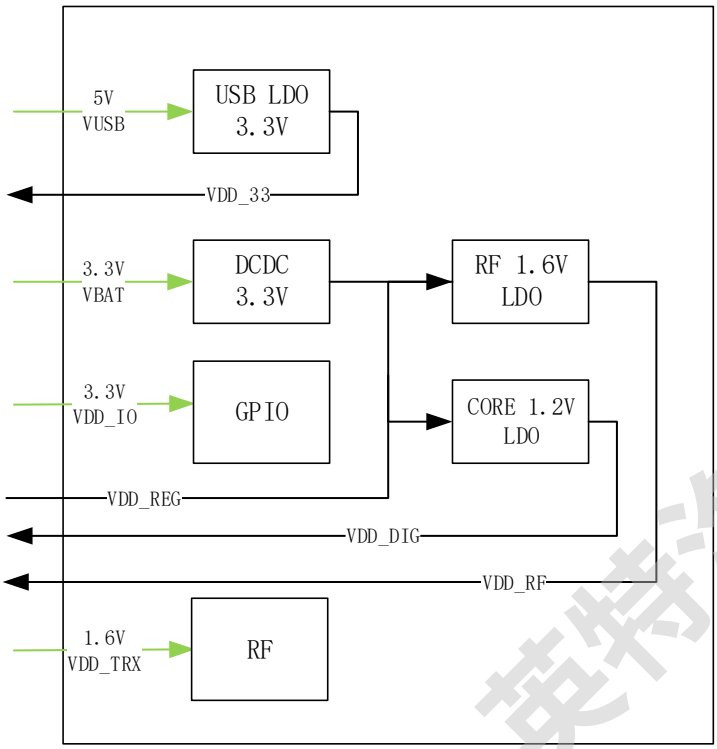

Figure 5 BR8654A02 Power DC

6.2. Temperature Limit Characteristics

Table 9 BR8654A02 Temp Characteristics

Parameters	Unit	Min	Max
Storage Temperature	°C	-55	+125
Ambient Operating Temperature	°C	-40	+125

6.3. Startup Signaling Sequence

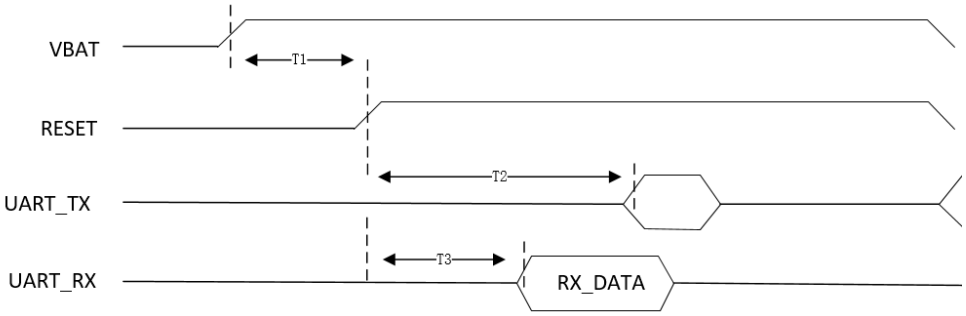

Figure 6 Startup Signaling Sequence

Table 10 Startup Timing

Item	Min	Type	Max	Unit
T1	5	-	-	ms
T2	20	-	-	ms
T3	10	-	-	ms

6.4. Digital IO DC Characteristics

BR8654A02 all GPIOs can configure as input pull up or input high resistor with system ctrl register. The GPIO pull up resistor typical is about 50KΩ.

Table 11 BR8654A02 IO DC Characteristics

Symbol	Parameter	Units	Min	Typical	Max
VIL	Low-level input voltage	V	-	0	0.9
VIH	High-level input voltage	V	2.0	3.3	-
VOL	Low-level output voltage	V	0	-	0.33
VOH	High-level output voltage	V	2.97	-	3.3
IOL	Low-level output current	mA	-	8	-

IOH	High-level output current	mA	-	8	-
Rpull	Pull up resistance	Ω	30K	50K	70K

6.5. RF Characteristics

Table 12 BR8654A02 RF Characteristics

Parameter	Conditions	Units	Min	Typical	Max
Frequency Range	-	MHZ	2400	-	2484
RX Sensitivity@1Mbps BLE	PER=30.8%	dBm	-70	-94	-
RX Sensitivity@2Mbps BLE	PER=30.8%	dbm	-70	-91	-
RX Sensitivity@Coded S=2 BLE	PER=30.8%	dbm	-70	-96	-
RX Sensitivity@Coded S=8 BLE	PER=30.8%	dbm	-70	-98	-
RX Sensitivity@1Mbps BT	BER=0.1%	dBm	-70	-90	-
RX Sensitivity@ EDR 2Mbps	BER=0.01%	dBm	-70	-92	-
RX Sensitivity@ EDR 3Mbps	BER=0.01%	dBm	-70	-85	-
Transmit Output Power	BR(GFSK)	dBm	-30	-	6
	EDR2(π/4-DQPSK)	dBm	-30	-	6
	EDR3(8-DPSK)	dBm	-30	-	6
	BLE	dBm	-30	0	6

6.6. Power Consumption

Table 13 BR8654A02 Power Consumption Characteristics (Average current)

Operation Mode	Unit	Min	Typical	Max
Deep Sleep	uA	-	10	-
Sleep	uA	-	400	-
Idle	mA	-	5.5	-

Operation Mode	Unit	DCDC			LDO		
		Min	Typical	Max	Min	Typical	Max
TX(SPP)	mA	-	6.8	-	-	9.5	-
RX(SPP)	mA	-	7.8	-	-	11.3	-
TX(BLE)	mA	-	7.5		-	10.3	-
RX(BLE)	mA	-	8.5		-	12.3	-

6.7. ESD

Table 14 ESD

Item	Voltage（V）	Current（mA）
HBM	2000	-
CDM	500	-
MM	100	-
LATCH UP	-	100

7. Reference circuit

7.1. Reference circuit with DCDC

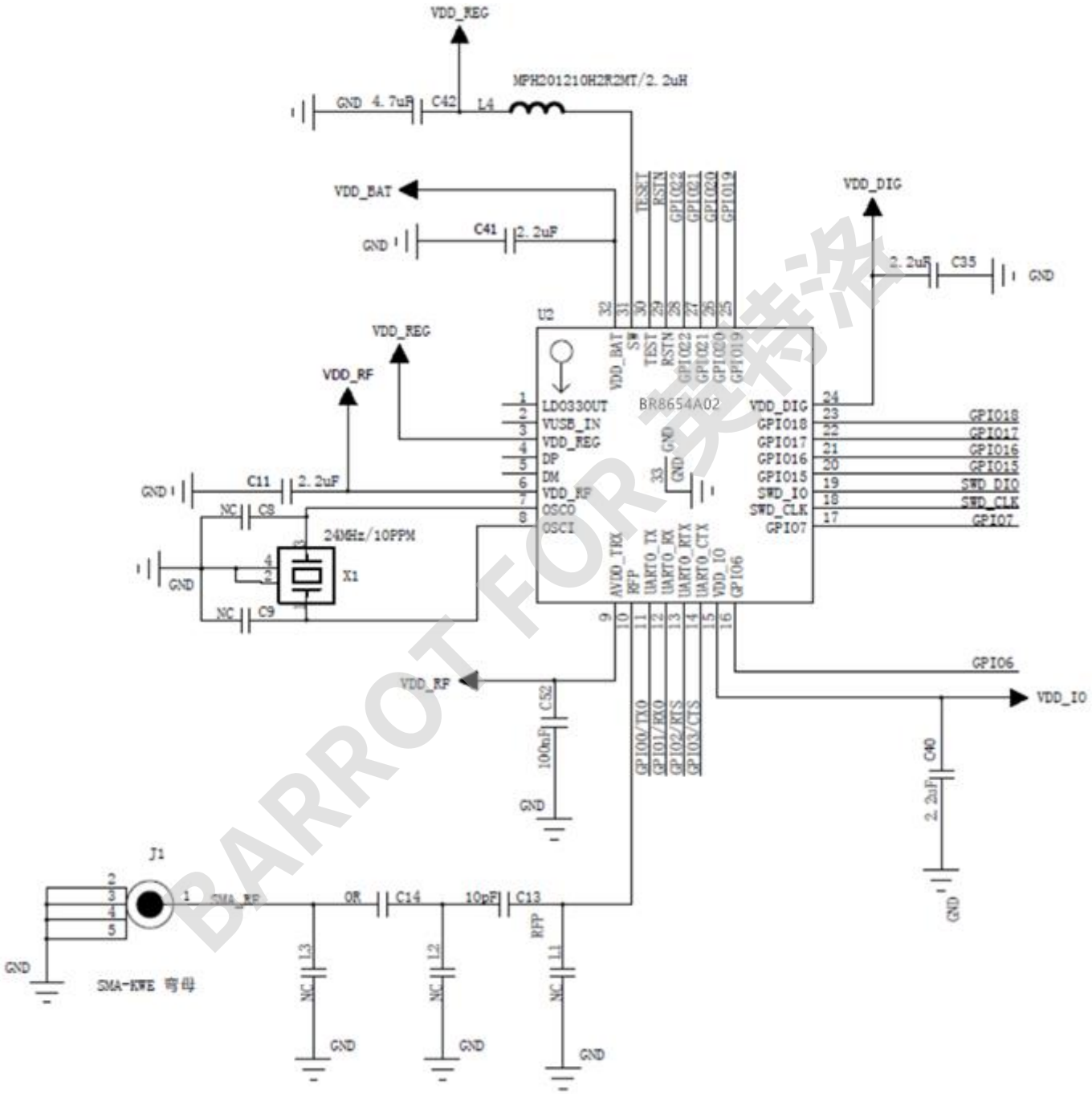

Figure 7 Reference circuit with DCDC

7.2. Reference circuit without DCDC

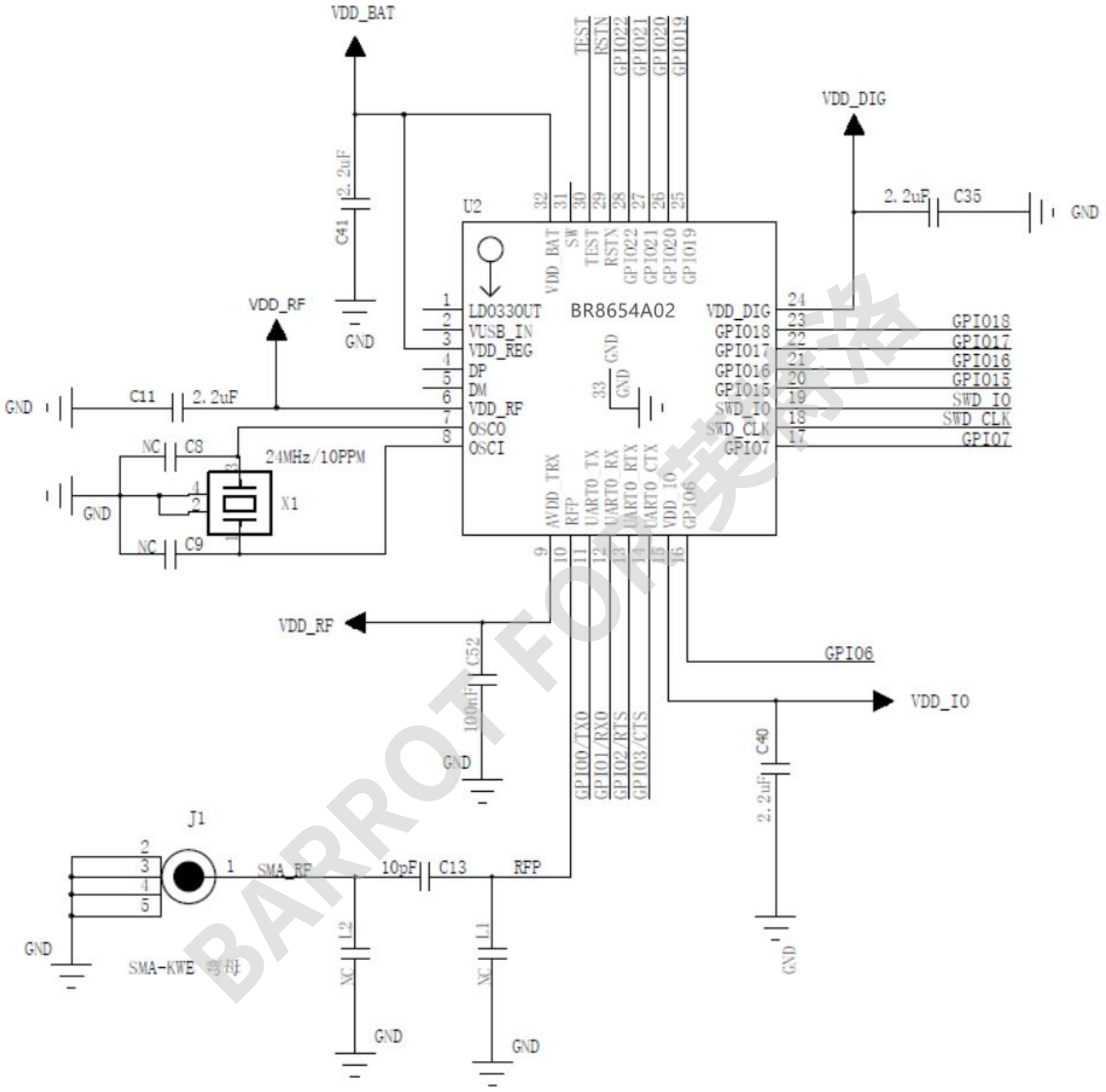

Figure 8 Reference circuit without DCDC

8. Package (QFN32L 5x5)

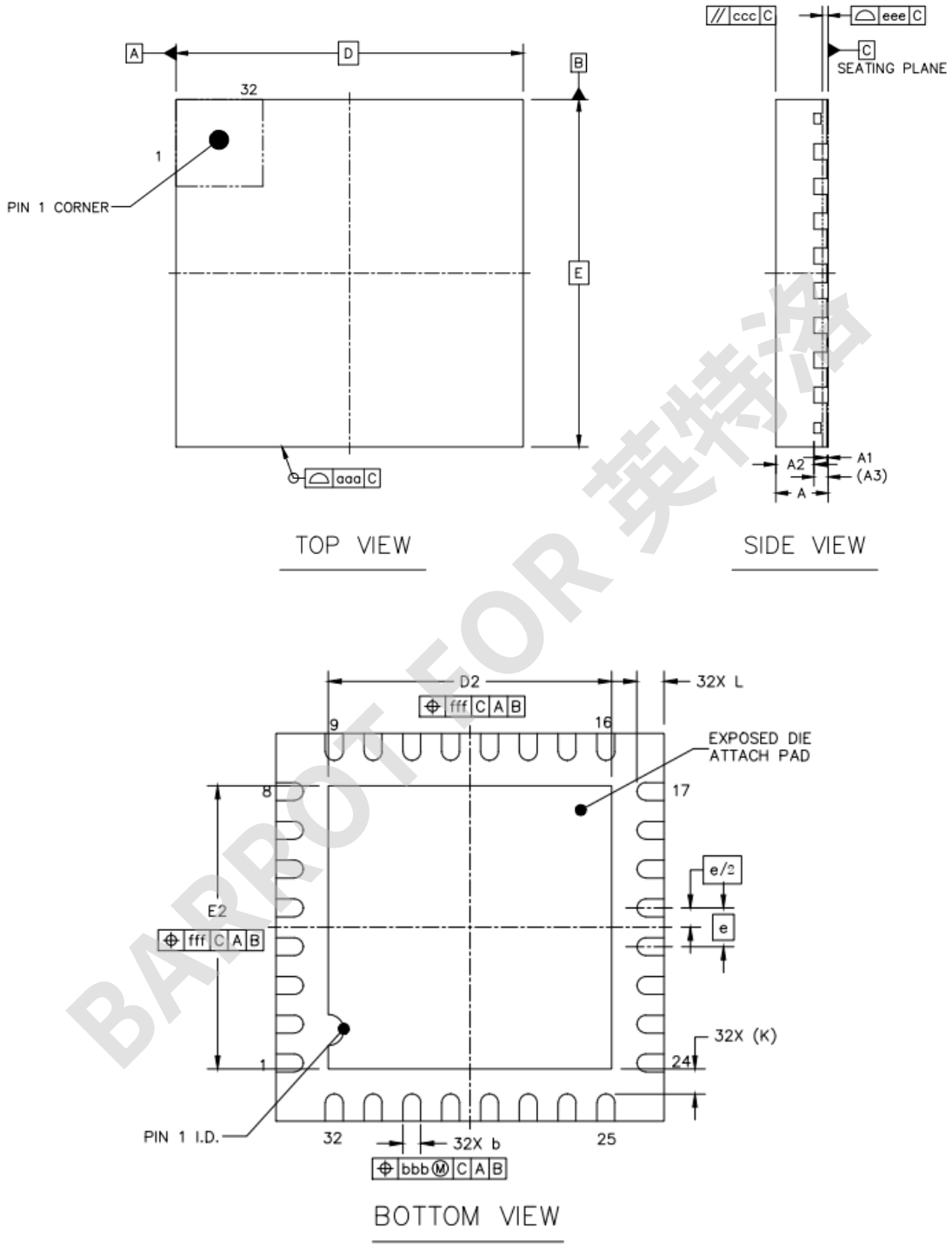

Figure 9 Package Dimension

Table 15 Package Dimension

Symbol	Millimeter		
	Min	Typical	Max
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.18	0.23	0.28
D	5 BSC		
E	5 BSC		
e	0.5BSC		
D2	3.6	3.65	3.7
E2	3.6	3.65	3.7
L	0.3	0.35	0.4
K	0.325 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		

9. MOQ

Package：Reel

The minimum number of packages: 5000pcs/ Reel, 4000pcs/Reel

10. Company Profile

Barrot Technology – Barrot is a world leading one-stop chipset level solution provider who offers wireless connectivity and audio intelligent hardware solutions featuring with own IPs. The company is an associated member of The Bluetooth SIG, and it is the only one who contributes to Bluetooth specification definition in Greater China. Barrot owns three high-tech IPs: Bluetooth RF, Bluetooth stack and Acoustic algorithms, so Barrot offers most integrated, robust, reliable, and easy-to-use wireless turn-key solutions for IOT, Automotive and Wireless audio applications.

Barrot devotes itself to being the most reliable short distance wireless technologies' solution provider in the world.

11. Contacts

总代理商：

深圳市英特洛智能有限公司

联系方式：

Email:william.lau@intelrow.tech

Tel:15361837696

12. Copyright